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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LI, AIMEE J	
ART UNIT	PAPER NUMBER
2183	3

DATE MAILED: 06/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/631,174	DWYER ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2000 and 02 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-19 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 2 August 2000.

Specification

3. The disclosure is objected to because of the following informalities: Please clarify or correct the drawing reference numbers 112 and 177 on page 11, lines 12, 14, 15, 17, and 19. It is unclear whether these numbers refer to these elements in Figures 3 and 4 or elements 52 and 75 in Figures 1 and 2, since it has not been indicated prior to these lines to refer to Figures 3 and 4 instead of Figures 1 and 2.

4. Appropriate correction or clarification is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being taught by Novak et al., U.S. Patent Number 5,809,522 (herein referred to as Novak).

7. Referring to claim 1, Novak has taught a computer system for efficiently executing instructions of computer programs, comprising:

a. Processing circuitry configured to execute instructions from one of a plurality of programs, said processing circuitry further configured to stop executing said one program during a first context switch in response to a first context switch command and to resume executing said one program during a second context switch in response to a second context switch command (Novak Abstract; column 8, lines 47-65; Figure 2; and Figure 5);

b. Cache memory (Novak Abstract; column 1, lines 12-17; and Figure 1);

c. Computer memory having a plurality of addresses (Novak Abstract; column 1, lines 12-17; columns 2-3, lines 61-16; and Figure 1); and

d. Memory control circuitry coupled to said processing circuitry, said memory control circuitry, in response to said second context switch command, configured to identify one of said addresses of said computer memory that is storing a data value previously used to execute an instruction of said one computer program prior to said first context switch, said memory control circuitry further configured to retrieve said data value from said computer memory in response to said second context switch command and to store said retrieved data value in said cache memory (Novak Abstract; columns 3-4, lines 56-4; column 4, lines 57-65; column 8, lines 13-65; Figure 1; Figure 2; and Figure 5).

8. Referring to claim 2, Novak has taught wherein said processing circuitry is further configured to execute instructions of another of said computer programs in response to said first context switch command (Novak Abstract; column 8, lines 47-65; Figure 2; and Figure 5).

9. Referring to claim 3, Novak has taught wherein said memory control circuitry is further configured to determine, in response to said second context switch command, whether said data value was utilized by said processing circuitry to execute an instruction within a specified time period prior to said first context switch (Novak Abstract; column 3, lines 38-52; column 8, lines 13-65; Figure 2; and Figure 5).

10. Referring to claim 4, Novak has taught wherein said memory control circuitry is configured to maintain a plurality of mappings, each of said mappings respectively correlating a data value stored in said cache memory with one of said memory addresses of said computer memory (Novak Abstract; column 4, lines 57-65; column 8, lines 13-65; Figure 2; and Figure 5), said memory control circuitry further configured to maintain a bit of information that is associated with one of said mappings, said memory control circuitry configured to assert said bit when a data value correlated with a computer memory address via said one mapping is utilized to execute an instruction of said one program, said memory control circuitry further configured to deassert said bit periodically (Novak Abstract; column 3, lines 38-51; column 8, lines 13-65; Figure 2; and Figure 5).

11. Referring to claim 5, Novak has taught wherein said memory control circuitry is further configured to determine, in response to said second context switch command arid based on said bit, whether said data value was recently utilized by said processing circuitry to execute an instruction prior to said first context switch (Novak Abstract; column 8, lines 13-65; Figure 2; and Figure 5).

12. Referring to claim 6, Novak has taught wherein said memory control circuitry is further configured to store said mappings and said bit to said computer memory in response to said first

context switch command and to retrieve said mappings and said bit from said computer memory in response to said second context switch command (Novak Abstract; column 3, lines 38-52; column 8, lines 13-65; Figure 2; and Figure 5).

13. Referring to claim 7, Novak has taught a computer system for efficiently executing instructions of computer programs, comprising:

a. Processing circuitry configured to execute instructions from one of a plurality of programs, said processing circuitry further configured to stop executing said one program during a first context switch in response to a first context switch command and to resume executing said one program during a second context switch in response to a second context switch command (Novak Abstract; column 8, lines 47-65; Figure 2; and Figure 5);

b. Cache memory (Novak Abstract; column 1, lines 12-17; and Figure 1);

c. Computer memory having a plurality of addresses (Novak Abstract; column 1, lines 12-17; columns 2-3, lines 61-16; and Figure 1); and

d. Memory control circuitry coupled to said processing circuitry, said memory control circuitry configured to maintain a plurality of mappings, said mappings respectively correlating data values stored in said cache memory with said memory addresses of said computer memory, said memory control circuitry configured to store said mappings in said computer memory in response to said first context switch command and to retrieve data values from said addresses that are identified by said mappings stored in said computer memory in response to said second context switch command, said memory control circuitry further

configured to store in said cache memory said retrieved data values (Novak Abstract; column 3, lines 38-51; columns 3-4, lines 56-4; column 4, lines 57-65; column 8, lines 13-65; Figure 1; Figure 2; and Figure 5).

14. Referring to claim 8, Novak has taught wherein said processing circuitry is further configured to execute instructions of another of said computer programs in response to said first context switch command (Novak Abstract; column 8, lines 47-65; Figure 2; and Figure 5).

15. Referring to claim 9, Novak has taught wherein said memory control circuitry is further configured to maintain utilization data indicative of which of said memory addresses are storing data values accessed within a specified time period prior to said first context switch (Novak Abstract; column 3, lines 38-52; column 8, lines 13-65; Figure 2; and Figure 5), and wherein said memory control circuitry, based on said mappings and said utilization data, is further configured to select for retrieval data values identified by one of said mappings and accessed within said specified time period (Novak Abstract; column 4, lines 57-65; column 8, lines 13-65; Figure 2; and Figure 5), wherein each of said retrieved data values is a data value selected by said memory control circuitry based on said utilization data (Novak Abstract; column 4, lines 57-65; column 8, lines 13-65; Figure 2; and Figure 5).

16. Referring to claim 10, Novak has taught wherein said memory control circuitry is farther configured to store said utilization data in said computer memory in response to said first context switch command and to retrieve said utilization data and said mappings in response to said second context switch command (Novak Abstract; column 3, lines 38-52; column 8, lines 13-65; Figure 2; and Figure 5).

17. Referring to claim 11, Novak has taught wherein said utilization data is a plurality of bits respectively associated with said mappings, wherein said memory control circuitry, for each data value accessed by said memory control circuitry, is configured to assert the bit associated with the mapping that correlates said each data value with one of said computer memory addresses, and wherein said memory control circuitry is configured to periodically deassert each of said plurality of bits (Novak Abstract; column 3, lines 38-52; columns 3-4, lines 56-4; column 4, lines 57-65; column 8, lines 13-65; Figure 2; and Figure 5).

18. Referring to claim 12, Novak has taught a method for efficiently executing instructions of computer programs, comprising the steps of:

a. Executing a plurality of computer programs in an interleaved fashion; switching which of said computer programs is being executed in said executing step (Novak Abstract; column 8, lines 47-65; and Figure 5);

b. Storing, prior to said switching step, at an address in computer memory a data value utilized in said executing step; identifying said address in response to said switching step (Novak Abstract; column 8, lines 47-65; and Figure 5);

c. Retrieving said data value from said address based on said identifying step and in response to said switching step (Novak Abstract; columns 2-3, lines 61-16; column 8, lines 13-65; Figure 2; and Figure 5);

d. Storing said retrieved data value in cache memory (Novak Abstract column 8, lines 13-65; Figure 2; and Figure 5); and

e. Retrieving said data value from said cache memory in response to said executing step (Novak Abstract; column 1, lines 12-17; columns 2-3, lines 61-38; and Figure 1).

19. Referring to claim 13, Novak has taught wherein said executing step further includes the step of executing instructions of a computer program in response to said switching step, and wherein said method further comprises the steps of:

a. Determining that said address is storing a data value previously utilized in said executing step to execute an instruction of said computer program (Novak Abstract and column 3, lines 38-52); and

b. Performing said identifying step based on said determining step (Novak Abstract; column 8, lines 13-65; Figure 2; and Figure 5).

20. Referring to claim 14, Novak has taught further comprising the steps of:

a. Correlating, respectively, data values stored in said cache memory with addresses of said computer memory (Novak Abstract; column 4, lines 57-65; column 8, lines 13-65; Figure 2; and Figure 5);

b. Asserting a bit each time a data value correlated with said address identified in said identifying step is accessed in response to said executing step (Novak Abstract; column 3, lines 38-51; column 8, lines 13-65; Figure 2; and Figure 5); and

c. Periodically deasserting said bit (Novak Abstract; column 3, lines 38-51; column 8, lines 13-65; Figure 2; and Figure 5).

21. Referring to claim 15, Novak has taught wherein said executing step further includes the step of executing instructions of a computer program in response to said switching step, and wherein said method further comprises the steps of:

a. Determining, based on said bit, that said address identified in said identifying step is storing a data value previously utilized in said executing step-to execute an instruction of said computer program (Novak Abstract; column 8, lines 13-65; Figure 2; and Figure 5); and

b. Performing said identifying step based on said determining step (Novak Abstract; column 8, lines 13-65; Figure 2; and Figure 5).

22. Referring to claim 16, Novak has taught a method for efficiently executing instructions of computer programs, comprising the steps of:

a. Executing instructions from a computer program (Novak Abstract; column 8, lines 13-65; Figure 2; and Figure 5);

b. Halting said executing step during a first context switch in response to a first context switch command (Novak Abstract; column 8, lines 47-65; Figure 2; and Figure 5);

c. Resuming said executing step during a second context switch in response to a second context switch command; maintaining a plurality of mappings (Novak Abstract; column 3, lines 38-51; columns 3-4, lines 56-4; column 4, lines 57-65; column 8, lines 13-65; Figure 1; Figure 2; and Figure 5);

d. Correlating, via said mappings, data values stored in a cache memory with memory addresses of computer memory outside of said cache memory; storing

said mappings in said computer memory in response to said first context switch command (Novak Abstract; column 4, lines 57-65; column 8, lines 13-65; Figure 2; and Figure 5);

e. Retrieving, based on said mappings and in response to said second context switch command, at least one data value from at least one of said addresses identified by said mappings; and storing said at least one retrieved data value in said cache memory (Novak Abstract; column 1, lines 12-17; columns 2-3, lines 61-16; column 8, lines 13-65; Figure 1; Figure 2; and Figure 5).

23. Referring to claim 17, Novak has taught further comprising the steps of:

a. Maintaining utilization data indicative of which of said memory addresses are storing data values accessed within a specified time period prior to said first context switch (Novak Abstract; column 3, lines 38-52; column 8, lines 13-65; Figure 2; and Figure 5); and

b. Selecting, based on said mappings and said utilization data, data values accessed within said specified time period (Novak Abstract; column 4, lines 57-65; column 8, lines 13-65; Figure 2; and Figure 5),

c. Wherein said retrieving step includes the step of retrieving each data value selected in said selecting step (Novak Abstract; column 4, lines 57-65; column 8, lines 13-65; Figure 2; and Figure 5).

24. Referring to claim 18, Novak has taught further comprising the steps of:

a. Storing said utilization data in said computer memory in response to said first context switch command (Novak Abstract; column 3, lines 38-52; column 8, lines 13-54; Figure 2; and Figure 5); and

b. Retrieving said utilization data and said mappings in response to said second context switch command (Novak Abstract; column 3, lines 38-52; column 8, lines 13-54; Figure 2; and Figure 5).

25. Referring to claim 19, Novak has taught wherein said utilization data is a plurality of bits respectively associated with said mappings, and wherein said method further comprises the steps of:

a. Asserting each of said bits associated respectively with each of said mappings that identifies a data value accessed in response to said executing step (Novak Abstract; column 3, lines 38-52; columns 3-4, lines 56-4; column 4, lines 57-65; column 8, lines 13-65; Figure 2; and Figure 5); and

b. Periodically deasserting each of said bits (Novak Abstract; column 3, lines 38-52; columns 3-4, lines 56-4; column 4, lines 57-65; column 8, lines 13-65; Figure 2; and Figure 5).

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Gulsen, U.S. Patent Number 5,727,211, has taught a multi-threaded system which stores cache information during a context switch.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

June 2, 2003

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